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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/671,436	09/27/2000	Yoshinari Matsuda	09792909-0425	6069
	7590 10/18/2007 EIN NATH & ROSEN	EXAMINER		
P.O. BOX 061080			LEVI, DAMEON E	
WACKER DRIVE STATION, SEARS TOWER CHICAGO, IL 60606-1080		STOWER	ART UNIT	PAPER NUMBER
			2841	
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			10/18/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

<b>↓</b>						
	Application No.	Applicant(s)				
	09/671,436	MATSUDA ET AL.				
Office Action Summary	Examiner	Art Unit				
	Dameon E Levi	2841				
The MAILING DATE of this communication app Period for Reply	ears on the cover s	heet with the correspondence address				
A SHORTENED STATUTORY PERIOD FOR REPLY THE MAILING DATE OF THIS COMMUNICATION.  - Extensions of time may be available under the provisions of 37 CFR 1.13 after SIX (6) MONTHS from the mailing date of this communication.  - If the period for reply specified above is less than thirty (30) days, a reply - If NO period for reply is specified above, the maximum statutory period of the period for reply within the set or extended period for reply will, by statute - Any reply received by the Office later than three months after the mailing earned patent term adjustment. See 37 CFR 1.704(b).  Status	36(a). In no event, howevery within the statutory minim will apply and will expire SI, cause the application to b	er, may a reply be timely filed  um of thirty (30) days will be considered timely.  X (6) MONTHS from the mailing date of this communication. ecome ABANDONED (35 U.S.C. § 133).				
1) Responsive to communication(s) filed on <u>07/1</u>	10/2007(Response	<u>.</u>				
2a) This action is <b>FINAL</b> . 2b) ☑ Th	is action is non-fin	al.				
3) Since this application is in condition for allows closed in accordance with the practice under Disposition of Claims						
4)⊠ Claim(s) <u>1-6 and 8-20</u> is/are pending in the application.						
4a) Of the above claim(s) is/are withdrawn from consideration.						
5) Claim(s) is/are allowed.						
6)⊠ Claim(s) <u>1-6,8-20</u> is/are rejected.						
7) Claim(s) is/are objected to.						
8) Claim(s) are subject to restriction and/o	r election requirem	ent.				
Application Papers		•				
9) The specification is objected to by the Examiner.						
10)⊠ The drawing(s) filed on <u>27 September 2000</u> is/are: a)⊠ accepted or b)☐ objected to by the Examiner.						
Applicant may not request that any objection to th						
11) ☐ The proposed drawing correction filed on is: a) ☐ approved b) ☐ disapproved by the Examiner.						
If approved, corrected drawings are required in reply to this Office action.						
12) The oath or declaration is objected to by the Examiner.						
Priority under 35 U.S.C. §§ 119 and 120		•				
13) 🛛 Acknowledgment is made of a claim for foreigi	n priority under 35	U.S.C. § 119(a)-(d) or (f).				
a)⊠ All b)□ Some * c)□ None of:		•				
1. Certified copies of the priority documents have been received.						
2. Certified copies of the priority documents have been received in Application No						
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)). * See the attached detailed Office action for a list of the certified copies not received.						
14) Acknowledgment is made of a claim for domest	ic priority under 35	U.S.C. § 119(e) (to a provisional application).				
a) ☐ The translation of the foreign language pro 15)☐ Acknowledgment is made of a claim for domes						
Attachment(s)						
1) Notice of References Cited (PTO-892) 2) Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) Information Disclosure Statement(s) (PTO-1449) Paper No(s)	5) 🔲	Interview Summary (PTO-413) Paper No(s) Notice of Informal Patent Application (PTO-152) Other:				

### **DETAILED ACTION**

#### **NEW GROUNDS OF REJECTION**

# PREVIOUS OFFICIAL ACTION WITHDRAWN

Applicant's arguments, as well as, Perfecting of a Claim for Priority filed 07/10/2007, with respect to the rejection(s) of the claim(s) with respect to Ishikawa et al US Patent 6339197 under 35 USC 103(a) have been fully considered and are persuasive.

Therefore, the Ishikawa et al reference, and hence, the previous non final rejection of 04/10/2007 has been withdrawn. However, upon further consideration, a new non final rejection is made in view of the newly cited prior art (Ishikawa et al US Patent 5243142).

# Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-6, and 8 are rejected under 35 U.S.C. 103(a) as being as being unpatentable over Ishikawa et al US Patent 5243142 in view of Yamazaki et al US Patent 5834327.

Regarding claim 1, Ishikawa et al discloses a printed circuit board comprising:
a glass substrate( element 1, Figs 1-6) provided with through-holes( element 3, Figs 1-6), conductive patterns( element 4, Figs 1-6) provided on both surfaces of the glass

substrate in such a manner as to be made conductive to each other via the throughholes, and a sealing member (element 5, Figs 1-6) provided to fill the through holes, the sealing member being operable to inhibit moisture permeation through the through holes.

Page 3

Ishikawa et al does not expressly disclose the glass substrate having a sealed side surface facing the portion to be sealed from moisture and an exposed side surface; or, the conductive patterns on said sealed side surface being connected to at least one display element.

Yamazaki et al discloses a device comprising a glass substrate(element 731, Figs 15A-16D) having a sealed side surface facing a portion to be sealed from moisture and an exposed side surface(column 17, lines 43-60, Figs 15A-16D);

and, the conductive patterns(elements 748, Figs 15A-16D)on said sealed side surface being connected to at least one display element(element 749, Figs 15A-16D). Accordingly, it would have been obvious to one of ordinary skill in the art, at the time the

invention was made to have included a sealed side surface and an exposed side surface, as well as, to connect the conductive patterns to a display element as taught by Yamazaki et al in the display device of Ishikawa et al for the purpose of providing a sealed in atmosphere, as well as, to electrically connect the display element to the substrate.

Regarding claim 2, Ishikawa et al discloses wherein the glass substrate is a no-alkali glass substrate( element 1, Figs 1-6).

Application/Control Number: 09/671,436

Art Unit: 2841

Regarding claim 3, Ishikawa et al discloses wherein the sealing member is a conductive paste containing an epoxy resin as a binder( element 5, Figs 1-6).

Regarding claim 4, Ishikawa et al discloses wherein a conductive film is provided on an inner wall surface of each of the through-holes in such a manner as to connect the conductive patterns provided on both surfaces of the glass substrate to each other, and an inner space, inside the conductive film, of the through-hole is filled with the sealing member (element 1,5,4, Figs 1-6).

Regarding claim 5, Ishikawa et al discloses wherein the sealing member is an epoxy resin( element 5, Figs 1-6)

Regarding claim 6, Ishikawa et al discloses wherein the surface of the sealing member exposed from each of the through-holes is covered with a metal film (element 6, Figs 1-6).

Regarding claim 8, Ishikawa et al discloses wherein each of said conductive patterns has a stacked structure of an epoxy resin film and a copper film formed thereon ( element 5,6, Figs 1-6).

Claims 9-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishikawa et al US Patent 6339197 in view of Yamazaki et al US Patent 5834327, Stevens US Patent 6392356 and further in view of Nakazawa et al US Patent 6411349

Regarding claim 9, Ishikawa et al discloses a device comprising:

Art Unit: 2841

a printed wiring board including a glass substrate( element 1, Figs 1-6) provided with through-holes( elements 3, Figs 1-6),

conductive patterns( elements 6, Figs 1-6) provided on both surfaces of the glass substrate in such a manner as to be made conductive to each other via the through holes, and a first sealing member( element 5, Figs 1-6) provided to fill the throughholes;

Yamazaki et al discloses a device comprising a glass substrate(element 731, Figs 15A-16D) having a sealed side surface facing a portion to be sealed from moisture and an exposed side surface(column 17, lines 43-60, Figs 15A-16D);

and, the conductive patterns(elements 748, Figs 15A-16D)on said sealed side surface being connected to at least one display element(element 749, Figs 15A-16D).

- a display device provided on one surface of the printed wiring board in such a manner as to be connected to a conductive pattern provided on a one surface of a printed wiring board (elements 30, Fig 3)
- a drive component for driving the display device, the drive component being disposed on the exposed surface of the printed wiring board in such a manner as to be connected to the conductive pattern provided on the other surface of the printed wiring board (elements 70,72, Figs 1-3, see column 5, lines 5-25)

Nakazawa et al discloses a display device assembly wherein

Stevens et al discloses a display device assembly comprising

• a second sealing member provided in such a manner as to surround a display

Application/Control Number: 09/671,436

Art Unit: 2841

device while being in contact with a printed wiring board and a protective glass board (element 252, Fig 12)

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included the glass circuit board with a sealed side surface and an exposed side surface and to connect the conductive patterns to a display element as taught by Ishikawa et al and Yamazaki et al for the purpose of providing a sealed in atmosphere, as well as, to electrically connect the display element to the substrate and also to arrange the display device components as taught by Stevens for the purpose of achieving a denser array of driver components in order to increase pixel pitch in the display device and additionally to add the second sealing member as taught by Nakazawa et al for the purpose vacuum sealing the display device assembly as a whole.

**Regarding claim** 10, Ishikawa et al disclose the instant wherein the glass substrate is a no-alkali glass substrate( element 1, Figs 1-6).

Regarding claim 11, Ishikawa et al discloses wherein the sealing member is a conductive paste containing an epoxy resin as a binder (element 5, Figs 1-6).

Regarding claim 12, Ishikawa et al discloses wherein a conductive film is provided on an inner wall surface of each of the through-holes in such a manner as to connect the conductive patterns provided on both surfaces of the glass substrate to each other, and an inner space, inside the conductive film, of the through-hole is filled with the sealing member (elements 3,5 Figs 1-6).

Application/Control Number: 09/671,436

Art Unit: 2841

Regarding claim 13, Ishikawa et al discloses wherein the sealing member is an epoxy resin( element 5, Figs 1-6).

Regarding claim 14, Ishikawa et al discloses wherein the surface of the sealing member exposed from each of the through-holes is covered with a metal film (element 6, Figs 1-6).

Regarding claim 15, Ishikawa et al discloses a device comprising:

a printed wiring board including a glass substrate( element 1, Figs 1-6) provided with through-holes( elements 3, Figs 1-6), conductive patterns ( elements 6, Figs 1-6) provided on both surfaces of the glass substrate in such a manner as to be made conductive to each other via the through holes, and a first sealing member( element 5, Figs 1-6) provided to fill the through-holes;

Yamazaki et al discloses a device comprising:

a glass substrate(element 731, Figs 15A-16D) having a sealed side surface facing a portion to be sealed from moisture and an exposed side surface(column 17, lines 43-60, Figs 15A-16D); and, the conductive patterns(elements 748, Figs 15A-16D)on said sealed side surface being connected to at least one display element(element 749, Figs 15A-16D).

Stevens et al discloses a display device assembly comprising

 bumps provided on a conductive pattern provided on one surface of a printed wiring board; a protective glass board disposed in such a manner as to face to the one surface of the printed wiring board; a display device provided on the Art Unit: 2841

surface, facing to the printed wiring board, of the protective glass board in such a manner as to be connected to the bumps (elements 60,12,30 Fig 3)

 a drive component for driving the display device, the drive component being disposed on the exposed surface of the printed wiring board in such a manner as to be connected to the conductive pattern provided on the other surface of the printed wiring board( elements 70,72, Figs 1-3, see column 5, lines 5-25)

Nakazawa et al discloses a display device assembly wherein:

 a second sealing member is provided in such a manner as to surround a display device while being in contact with a printed wiring board and a protective glass board (element 252, fig 12)

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included the glass circuit board with a sealed side surface and an exposed side surface and to connect the conductive patterns to a display element as taught by Ishikawa et al and Yamazaki et al for the purpose of providing a sealed in atmosphere, as well as, to electrically connect the display element to the substrate and also to arrange the display device components as taught by Stevens for the purpose of achieving a denser array of driver components in order to increase pixel pitch in the display device and additionally to add the second sealing member as taught by Nakazawa et al for the purpose vacuum sealing the assembly as a whole.

**Regarding claim** 16, Ishikawa et al disclose the instant wherein the glass substrate is a no-alkali glass substrate ( element 1, Figs 1-6)

Art Unit: 2841

Regarding claim 17, Ishikawa et al discloses wherein a conductive film is provided on an inner wall surface of each of the through-holes (elements 3, Figs 1-6) in such a manner as to connect the conductive patterns provided on both surfaces of the glass substrate to each other, and an inner space inside the conductive film, of the through-hole is filled with the sealing member (element 5, Figs 1-6).

Regarding claim 18, Ishikawa et al discloses wherein the sealing member is an epoxy resin( element 5, Figs 1-6).

Regarding claim 19, Ishikawa et al discloses wherein the surface of the sealing member exposed from each of the through-holes is covered with a metal film (element 6, Figs 1-6).

Regarding claim 20, Ishikawa et al discloses wherein the surface of the sealing member exposed from each of first sealing member exposed from each of the throughholes is covered with a metal film (element 3,6, Figs 1-6).

## Response to Arguments

Applicant's arguments, with respect to the rejection(s) of claim(s) 1-6, and 8-20 (submitted 07/10/2007) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made above.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dameon E. Levi whose telephone number is (571) 272-

Application/Control Number: 09/671,436 Page 10

Art Unit: 2841

2105. The examiner can normally be reached on Mon.-Thurs. (9:00 - 5:00) IFP, Fridays Telework.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Diego Gutierrez can be reached on (571) 272-2245. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Dameon E Levi

Examiner

Art Unit 284

DEL

10/14/07